

U.S. Department of Commerce, Patent and Trademark				Atty. Docket No.		Application No.	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				SNDK.272US0		10/002,696	
				Applicants		Conf. No.	
Use several sheets if necessary)				Eliyahou Harari et al.		4652	
				Filing Date		Art Group	
				October 31, 2001		2814	

U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
<i>[Signature]</i>	1	5,912,844	6/15/1999	Chen et al.			

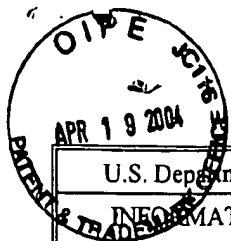
U.S. Published Patent Application Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate

Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)		

Examiner <i>[Signature]</i>	Date Considered <i>9/13/04</i>
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	1	3,979,582	9/7/1976	Mims			
	2	4,057,788	11/8/1977	Sage			
	3	5,311,049	5/10/1994	Tsuruta			
	4	5,539,690	7/23/1996	Talreja et al.			
	5	6,670,669	12/30/2003	Kawamura			
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		Document	Date	Country	Class	Subclass	Yes	No
	8	58-102394	17/6/1983	Japan			X	
	9	WO01/13378A1	22/2/2001	WIPO			Abstract	X

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	10	Krick, P.J., "Dual-Level Sense Scheme for Composite Insulator Memory Arrays", IBM technical Disclosure Bulletin, Vol. 17, No. 6, November 1974, pp. 1811-1813.
	11	Lai, S.K. et al., "Comparison and Trends in Today's Dominant E2 Technologies", IEEE, IEDM 86, 1986, pp. 580-583.
	12	Examiner Jennifer M. Dolan, Office Action dated April 5, 2004, United States Patent and Trademark Office, Application No. 10/161,235, 19 pages.

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Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
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<i>[Signature]</i>	7	6,677,200 B2	1/13/2004	Lee et al.			
<i>[Signature]</i>	8	6,580,120 B2	6/17/2003	Haspeslagh			

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<i>[Signature]</i>	9	2003/0134476A1	7/17/2003	Roizin et al.			
<i>[Signature]</i>	10	2003/0209754A1	11/13/2003	Haspeslagh			
<i>[Signature]</i>	11	2002/0196665A1	12/26/2002	Kim			

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<i>[Signature]</i>	12	Luc Haspeslagh, "Two Bit Non-Volatile Electrically Erasable and Programmable Memory Structure, a Process for Producing Said Memory Structure and Methods for Programming and Erasing Said Memory Structure", Provisional Application 60/296,618, filed June 7, 2001, priority claimed by US 6,580,120.

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	19	2003/0081460A1	5/1/2003	Choi et al.			
	20	2003/0016561A1	1/23/2003	Lee et al.			
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